Development of millimeter and submillimeter-wave local oscillator circuits for a space telescope

(Invited)

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ABSTRACT

FIRST (Far InfraRed and Submillimetre Telescope) is a European science mission that will perform photometry and spectroscopy in the 80-670 µm range. The proposed heterodyne instrument for FIRST is a seven channel receiver which combines the high spectral resolving capability (0.3-300km/s) of the radio heterodyne technique with the low noise detection offered by Superconductor-Insulator-Superconductor (SIS) and Hot Electron Bolometer (HEB) mixers. It is designed to provide almost continuous frequency coverage from 480-2700 GHz. The Jet Propulsion Laboratory is responsible for developing and implementing the local oscillator sources for the highly sensitive mixers. The present state-of-the-art approach for millimeter-wave multipliers, based on waveguide blocks and discretely mounted devices, becomes harder and harder to implement as the frequency range is extended beyond 300 GHz. This talk will focus on the technology that is being developed to enhance and extend planar integrated Schottky devices and circuits to meet mission local oscillator requirements. The baseline approach is to use GaAs power amplifiers from 71 to 115 GHz followed by a series of planar Schottky diode varactor multiplier stages to generate the required LO signal. The circuits have to be robust, relatively easy to assemble, and must provide broad fix-tuned bandwidth. A number of new technology initiatives being implemented to achieve these goals will be discussed. Approaches include quartz-based and substrate-less diode circuitry and integrated GaAs membrane technology. Recent results and progress-to-date will be presented.

1. INTRODUCTION

High-resolution millimeter and sub-millimeter heterodyne observations allow for a better understanding of physical phenomena present in the universe [1]. Far InfraRed and Submillimetre Telescope (FIRST) is a European mission with an American contribution where the objective is to study the formation and evolution of galaxies in the early universe and the formation of stars and the physics of the interstellar medium (and the interaction between the two) [2]. Such observations are severely limited by the atmosphere and can only be done in airborne or space borne platforms. FIRST will be launched in 2007 and will be based in the L2 orbit. A recent overview of the mission is presented in [3].

The heterodyne instrument on FIRST is based on 7 distinct receiver channels. Five pairs of fixed tuned double side-band SIS mixers in dual polarization cover 480-1250 GHz (625-240 um) region with a specified system noise temperature of 70-500 K. Two HEB (Hot Electron Bolometer) mixers are expected to cover 1410-1910 GHz (213-157 um) and 2400-2700 GHz (125-111 um) with a noise temperature of 650-800 K. The low noise temperature expected from these receivers will allow for very high-resolution spectroscopy.

The required local oscillator sources to pump these mixers continue to be a critical factor towards the successful implementation of the mission. The goal of the technology development for the LO system for FIRST is to enable solid state sources into the THz range with enough output power to pump the mixer. Based on the science requirements the goal of the LO development effort is to provide continuos frequency coverage from 480 to 1250 GHz and then two bands at 1410-1910 and 2400-2700 GHz. The frequency stability accuracy of 1 part in 10^8 is desired with sufficient output power to pump the mixer. The LO system should also provide for frequency switching for side band de-convolution. A modular design to reduce cost and simplify implementation is thus quite appropriate. The US contribution is based on the three highest frequency receivers while the remaining receivers will be developed and built by the European consortium. This paper will

focus on the ongoing effort at the Jet Propulsion Laboratory to develop and demonstrate enabling technology that will make possible the local oscillators for bands 5, 6 and 7. Table 1 depicts the seven frequency bands proposed for FIRST along with required LO powers necessary for successful mixing operation for the three highest bands as suggested by the FIRST Mixer Working group [4].

LOCAL OSCILLATOR BANDS FOR FIRST

Initial bands	71-79 GHz	80-92 GHz	88-99 GHz	92-106 GHz	106-112.5 GHz
x2	142-158	160-184	176-198	184-212	212-225
x2 x2	284-316	320-368	352-396	368-424	424-450
x2 x3		480-552 Band 1a		552-636 Band 1b	
x2 x2 x2		640-736 Band 2a	704-792 Band 2b	736-848 Band 3a	848-900
x2 x2 x3	852-948 Band 3b	960-1104 Band 4a	1056-1188 Band 4b	**1104-1272 Band 5 (36 μW)**	1272-1350
x2 x2 x2 x2			**1408-1584 Band 6a (1.2 μW)**		
x2 x2 x3 x2	**1704-1896 Band 6b (1.2 μW)**			**2400-2544 Band 7a (1.2 μW)**	**2544-2700 Band 7b (1.2 μW)**

Table 1: Proposed local oscillator bands for FIRST. The required power levels assume a 27% diplexer coupling and a 50% margin on the power levels required at the focal plane unit [4]. For Bands 6 and 7 single polarization is assumed.

2. TECHNOLOGY ROADMAP

There has been considerable interest and advancement towards making planar Schottky diode multipliers in the last few years, however, the required performance specifications (both in power and bandwidth) for the FIRST LO sources remain rather challenging. The highest frequency multiplier circuit reported to date is a tripler to 1395 GHz, which produces about 16 microwatts of power with a input power of 7 mW from a carcinotron source. The diode used in this multiplier is whisker contacted and the circuit is based on a waveguide block [5]. The highest frequency all solid state multiplier chains reported to date are around 1000 GHz (InP Gunn diode at 111.2 GHz followed by two whisker-contacted triplers) with output power of 60-120 microwatts [6].

On the other hand, balanced planar Schottky diode multipliers have been reported in to the 350 GHz range with about 5 mW of output power [7]. More remarkably it is now possible to design and build very high power multipliers in the 150-320 GHz range that can be used to drive next stage multipliers. 80 mW at 140 GHz, 76 mW at 180, and 15 mW at 270 have already been demonstrated and a number of slightly different approaches based on the balanced doubler concept have been demonstrated with very encouraging results [7,8,9].

These chains require very high power IMPATT sources around w-band instead of the traditionally used Gunn devices. The IMPATT sources can produce in excess of 400 mW in the W-band range however they have a very limited tuning bandwidth and inferior noise characteristics to Gunn diodes. In order to obtain multiplier chains to 2500 GHz it becomes essential to pump the earlier stages with significant amount of power and it is highly desirable to have primary sources that are tunable in order to meet the bandwidth criteria imposed by the FIRST mission. To address these concerns and based on the recent spectacular results from HEMT-based MMIC power amplifiers, the primary source on FIRST will be a low-noise, low-power (i.e. YIG or DRO based) source followed by MMIC power amplifiers. Power amplifiers will be used to as high a frequency as possible, and, by utilizing power combining techniques, sufficient power will be available at W-band to enable the required output power at the very high frequencies. It is important to ensure that the use of power amplifiers will not add

extra noise in the LO chain since the multiplication factor for the highest chain is 24 and phase noise increases as 20log(n) where n is the multiplication factor. Section 2.1 will briefly discuss the recent performance of MMIC amplifiers.

Each multiplier circuit consists of two rather entwined components – the nonlinear solid state device and the circuit that enables the frequency conversion. To successfully meet the challenge of this particular task it is important to further refine and advance both of these critical aspects. As the frequency increases and all concerned dimensions shrink, it often becomes difficult to separate the device from the circuit. However, distinct processes, procedures and technologies must be developed to optimize each component individually along with a global scheme of simulation, monolithic integration, and assembly that can result in robust high performance components. Section 2.2 will discuss the recent progress towards making high frequency Schottky diodes while Section 2.3 will discuss recent performance of a fix tuned 200 GHz multiplier stage. Section 2.4 will then elaborate on the on-going efforts towards higher frequency implementations.

2.1   State-of-the art GaAs-based Power Amplifiers

A major hurdle towards the development of very high frequency multipliers has been the lack of high power viable sources as the drivers. Gunn devices because of their low-noise behavior have been the favorite pump sources for almost all heterodyne systems that have flown to date. However, commercial GaAs Gunns can only put out about 100 mW at 100 GHz, though state-of-art InP Gunns can put out as much as 200 mW at 103 GHz [10]. Recent advances in the upper frequency limit and output power of three terminal devices have now made it possible to consider them as an alternative to fundamental oscillator sources [11-13]. 50 micron thick substrate, 0.1 micron InGaAs/AlGaAs high electron mobility transistor (HEMT) technology has now yielded state-of-the-art MMIC power amplifiers at W-band that have output power as high as 0.35W [13]. Use of InP promises [14] even more efficiency though currently the GaAs technology has been base-lined for FIRST. Use of power amplifiers in a LO chain, however, raises questions about the noise contributions of the amplifier to the receiver by means of the LO injected signal. This issue was examined in Reference 15.

Briefly, a sensitive waveguide receiver at the Caltech submillimeter-wave observatory at Mauna Kea, Hawaii was utilized to make astronomical observations using a GaAs power amplifier in the multiplier chain. A 278 GHz SIS receiver [16] was used to observe the Methanol (CH_3OH) line in the Orion-South Nebula. The initial LO chain configuration is shown in Figure 1 (a). The Gunn was phase locked and a receiver noise temperature of 22.5 K +/- 1 K (double side band) was measured using hot and cold loads. The observation was done with an integration time of 400 seconds and a number of scans were taken for accuracy. The telescope was then pointed off the source for calibration and to get a measure of the noise floor. The MMIC amplifier was then inserted into the LO chain as shown in Figure 1 (b). The measured noise temperature of the receiver was 21.3 K +/- 1K double side band while keeping identical SIS current to the measurement with the Gunn diode. The same observation of the Orion Nebula with identical integration time and scans was carried out. There was no discernible line broadening and the noise floor in both cases was observed to be the same. This indicates that at least with a single tripler the phase noise added from the power amplifier is not significant. However, to truly reflect the nature of FIRST the Gunn diode should be replaced by a low phase noise DRO and a chain to much higher frequencies must be considered.

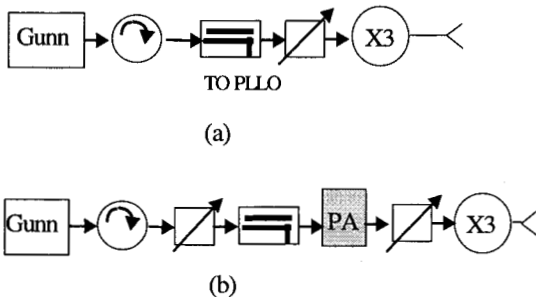
Gunn → TO PLLO → X3
(a)

Gunn → PA → X3
(b)

Figure 1: LO chain configuration at the CSO with and without the PA. A second isolator between the PA and the multiplier would have been desirable since some standing wave problems were observed. However given the mounting mechanics, we were unable to do so.

The most recent results achievable from GaAs power amplifiers specifically being developed for FIRST are being reported elsewhere [17]. Figure 2 shows the performance of the MMIC amplifiers that were designed to cover the 90 to 106 GHz frequency range. Over 200 mW of power is available at W-band from single-chip modules and it is possible to further increase this by power combining techniques that have been successful in the past [18].
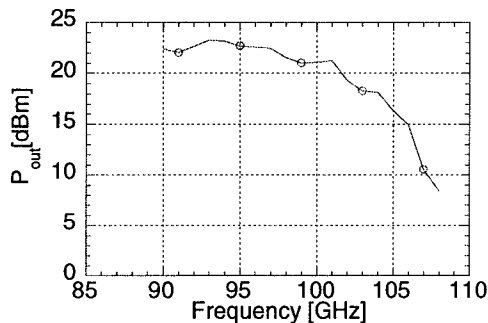
Figure 2. Output power as a function of frequency as obtained from 2 driver amp modules followed by one power amp module. An active multiplier chain based on a YIG oscillator is driving the amplifiers (Data courtesy of Lorene Samoska and Todd Gaier, JPL).

2.2   THz Planar Schottky Diodes

Whisker contacted Schottky diodes have been extensively used for frequency multiplication and are still used for applications above a few hundred GHz. However, recent advances in both the fabrication technology for planar Schottky diodes and the understanding of planar devices has enabled very efficient and high power planar Schottky diode circuits up to 350 GHz. The planar approach also offers a number of advantages such as robustness and multiple-diode circuits that are not easily possible with whisker contacted diodes. Researchers at the University of Virginia have successfully fabricated high performance planar Schottky diodes that work into the THz range. The Jet Propulsion Laboratory has built on this success by harnessing a number of advanced technologies to help with the fabrication of these device, since as the frequency increases some of the traditionally used technologies start becoming difficult to implement [19].

A representative device recently fabricated at JPL is shown in Figure 3. This is a 4-anode, 310 GHz, balanced doubler chip based on the design outlined in Reference 7. This particular chip is 480x160 microns and 50 microns thick. A close-up of the anode is shown in Figure 3(b). Note that the anode is made as a rectangular strip instead of the conventionally used circular anode. By using a rectangular shape the parasitic resistance can be reduced. In this particular device, the anodes have been made by using a 5x projection aligner and the anode size is 1.5x9.3 microns. The I-line stepper can make dimensions as small as 0.35 micron, but JPL's in-house electron beam lithography capability is better for geometries smaller than 1 μm. The mesa etching required for this particular chip was done by using reactive ion etching (RIE), which allows for much better control and repeatability as compared to wet chemical etching. Device separation was also done by RIE instead of the traditionally used high speed dicing procedures. The RIE allows us to space individual devices very close to each other and more importantly allows for the use of arbitrarily shaped chips. The devices are fabricated using standard 3-inch wafers. Thus, a successful run will result in hundredsto thousands of similar devices (depending on the mask and device size). The air-bridge part of the device is shown in more detail in Figure 3(c). This is obtained by using a thermally cured layer of photoresist that allows for the air-bridge to have the required curvature without breaking. Once the top side processing is completed the wafers are mechanically lapped down to 50 microns. Our initial wafers proceeded through backside processing as individual reticles (approximately 6 x 8 mm), but we expect that future runs will be handled as wafer quarters or full wafers in order to increase numerical yield.

2.3   Broadband Waveguide Circuits

The balanced doubler design has been shown to work quite well at least up to 320 GHz [7]. The doubler block designed for the 92-106 GHz bandwidth (this corresponds to the first stage multiplier for Band 5 in Table 1) is based on the design discussed in some detail for a lower frequency band [20]. The design and measured performance of this particular multiplier circuit will be discussed briefly. The varactor chip to be used for this circuit has been fabricated at University of Virginia and comprises of 6 anodes (3 anodes per leg). The epitaxial doping is 2.e17 and the breakdown is measured to be 9.5 volts for a 50 microamp current level. The series resistance is approximately 4 ohms per anode and the zero bias capacitance is approximately 49 fF. The embedding circuit comprises a quartz circuit where the varactor chip is mounted up-side-down on the quartz circuit which is then mounted on the split waveguide block. The lithographic process used to fabricate the quartz circuit results in a high degree of control over the circuit dimensions and thus significant control over the embedding impedance.

4

(a)
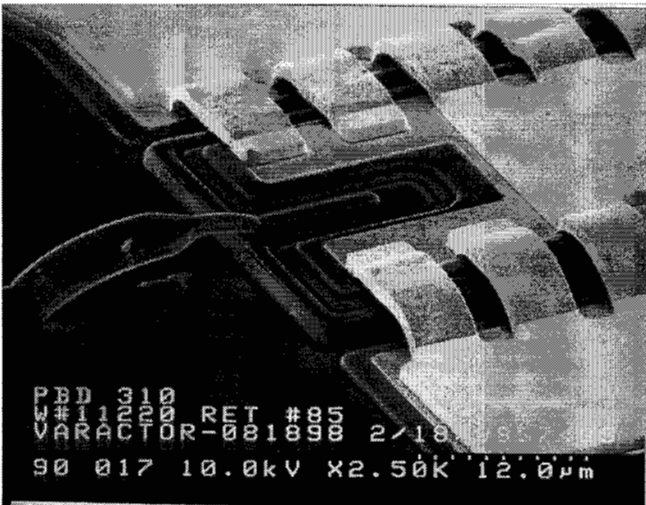
(b)
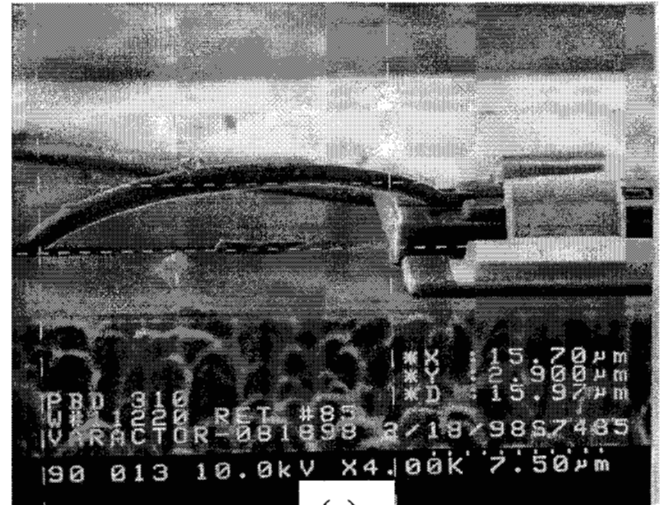
(c)

Figure 3 : A 4-anode 310 GHz balanced doubler chip.

The lower half of the split waveguide block is shown in Figure 4. The input waveguide (WR-10) and the output waveguide (WR-5) flanges are on opposite sides of the block and are offset by 0.3 inches. DC bias to the chip is provided through a SMA connector that is not shown in Figure 4. The 50 micron thick quartz circuit sits in a grove machined in the lower half of the block. The quartz circuit comprises an output embedding circuit, a probe for a microstirp-to-waveguide transition and a low-pass hammerhead filter for external DC bias. The assembly process is relatively simple. Two 1-mil soft gold bond wires are first attached to each of the outer bonding pads on the quartz structure. One additional bondwire is attached to the quartz structure past the hammerheads. This will be attached to the SMA connector before the two halves are assembled. The varactor chip is then soldered up-side-down on to the quartz structure. The quartz structure including the device is now placed in the lower half of the waveguide block and the 1-mil gold bondwires are attached to the waveguide block. The DC connection is now completed by tacking the bondwire on to the SMA center conductor. The two halves are now ready to be assembled.

5

The multiplier was divided up into a nonlinear active part modeling the behavior of the diodes, and a passive part modeling the rest of the circuit. A finite element electromagnetic simulator, Ansoft's High-frequency Structure Simulator (HFSS) was used to analyze the passive circuit elements, yielding scattering parameter matrices referred to the diode and waveguide ports. To simplify and speed up the process the passive circuitry was divided up into small elements at electromagnetically appropriate points, giving several S-parameter matrices. Ports were attached to probes on each anode so that the individual embedding impedances for each varactor could be monitored directly. More detailed embedding impedances simulations for this block have been presented in Reference [9]. The diodes were then embedded into the resulting cascaded S-parameter matrix blocks to determine the total efficiency and power performance of the multiplier.

The performance of this particular circuit is shown in Figure 5. A cascaded chain of three MMICs (two driver amplifiers followed by a power amplifier) were used followed by a low loss isolator to determine the fixed tuned bandwidth of the circuit with 100 mW of input power, Figure 5(a). It should be pointed out that the circuit was designed to operate optimally with about 150 mW of input power. The results indicate that a 3dB bandwidth of about 10 % is possible with a peak efficiency of 30 %. Figure 5(b) shows the power sweep results from the same circuit indicating that an efficiency of 35% is possible. All of these results were obtained at room temperature. The mission specifications allow for the multipliers to be cooled to 100 K which is expected to further improve the efficiency and output power of this multiplier circuit.
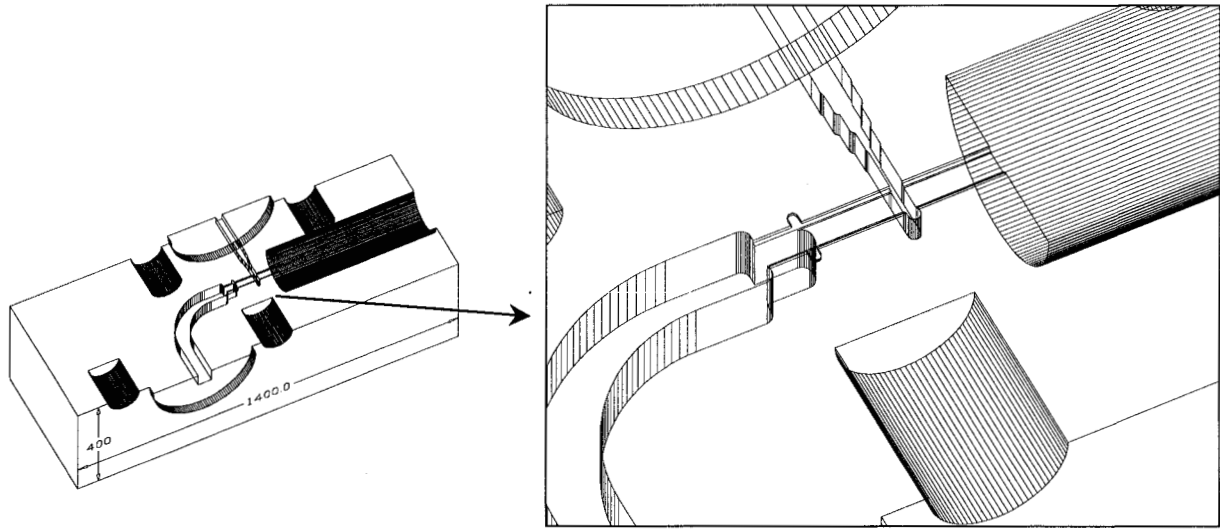

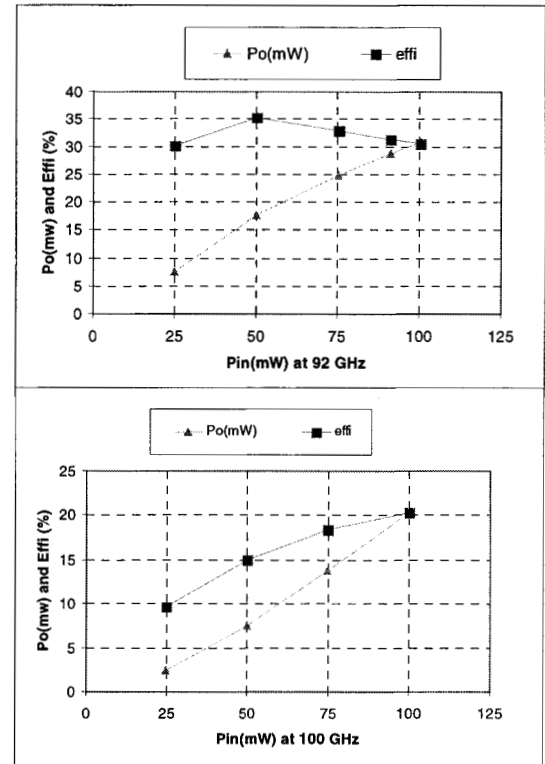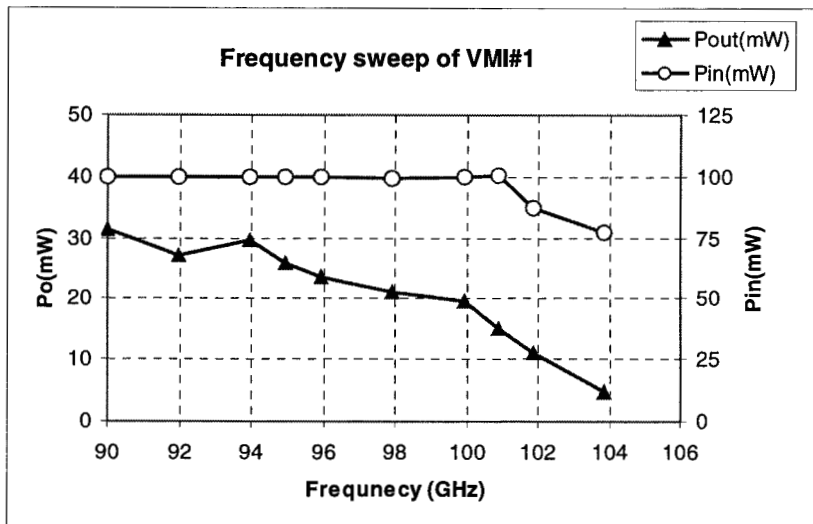**Figure 4: Waveguide block for the 200 GHz multiplier doubler.**

Figure 5: Measured performance of the 200 GHz multiplier.

[handwritten annotations:] Into Siegel related to Peters NIR
(A) - Directly related to Peters NIR
(B) - Directly Related

2.4   The Next Frontier

The results presented in this paper along with the other reported results with planar Schottky multipliers are encouraging. Earlier circuits based on the balanced doubler design used a mounting mechanism where the diode chip was directly soldered to the block and a precision machined coax structure was used to bias the chips. In Reference 9 a scheme where the diode is still soldered to the block but now a quartz substrate with the matching circuit is used to contact the diode chip was used. A third approach, the one that is being used in the current design, solders the diode chip directly to the quartz based filter which in turn is put into the waveguide block and wire bonds are used to contact the quartz circuit. A scheme of directly bonding the chip on to the block with a ribbon connecting the center conductor has been proposed and successfully used [21]. In spite of this success it is obvious that as the frequency of operation will increase most of these techniques would become very difficult to implement. The desired chip thickness at 300 GHz is already 38 microns and thinner chips would be harder to handle and routinely mount in waveguide blocks.

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In order to circumvent these limitations and implement technologies that can work well into the THz range we have proposed two novel ways of making the multiplier chips. In the first implementation, the matching circuit along with the device are fabricated on the epitaxial layer but after the front side processing is completed a backside procedure is initiated that removes all of the GaAs under the matching circuit. Only a 50 micron-thick GaAs frame is left around the matching structure and the Schottky anodes will be on one edge of this frame. This "substrateless" technology will result in no lossy material under the matching circuit (which could be a straight metal line) allowing for better matching conditions. The structure will be physically much bigger than the individual device, thus allowing easier handling of the structure. Moreover, beam leads will be placed on this structure that will allow for efficient heat transfer and an easier assembly procedure. Some representative passive structures have already been fabricated. One of such structures is shown in Figure 6.

In order to understand if such an implementation can work we have initiated extensive simulations based on structures such as the one shown in Figure 6.
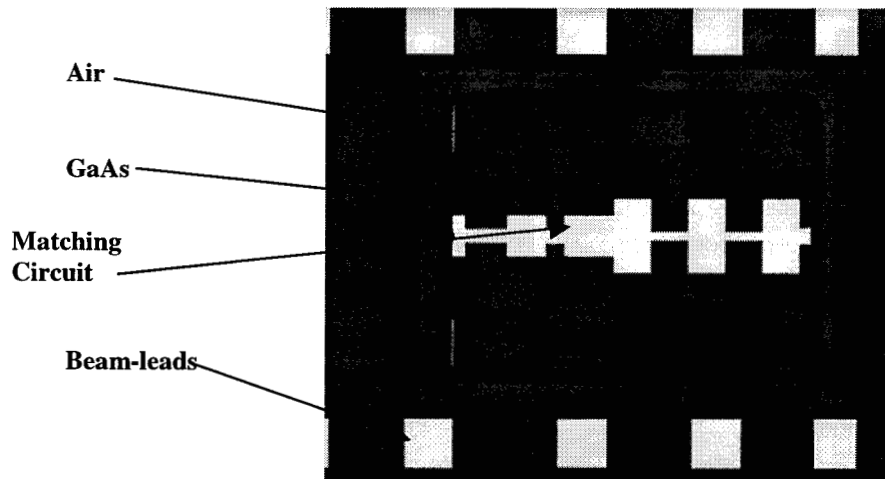
Figure 6: An example of the "substrateless" technology showing a matching circuit at 200 GHz. The shiny part is the Au metalization which is enclosed by a 50 micron thick and 50 micron wide GaAs frame. The devices will be implemented on the other side of the shown structure.

NEW?

A second approach that is under consideration for the very high frequency circuits is based on the successful implementation of Schottky diode mixers in the 2500 GHz range [22-23]. The major thrust of this technology is to develop and prototype monolithic multiplier circuits for the highest frequency (2.4-2.7 THz) bands. The approach utilizes novel GaAs MOMED (monolithic membrane diode) circuitry with integrated sub-micron Schottky barrier devices implemented in single and antiparallel-pair geometries for resistive tripling. The surrounding input/output circuitry is formed from high precision mechanically machined waveguide, made at first with electroformed metallic materials, and later with newly proposed MEMs (micro-electro-mechanical-structures) style semiconductor processing.
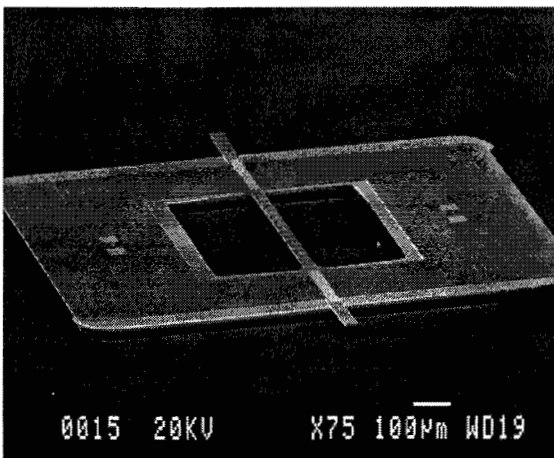

Figure 7: The 2.5 THz mixer circuit from [22].

3. SUMMARY

Building on the recent advancement in HEMT based power amplifiers and advanced integration technologies it is now possible to design and build planar multiplier stages in to the THz range. The power amplifiers will allow for very high power tunable sources and the goal for the lower stage multipliers will be to make them high power without sacrificing reliability. Higher frequency stages would have to be designed using some of sort of integration technique such that the semiconductor device is part of a bigger easier to handle structure. The local oscillator sources for FIRST will be challenging and require advancement in the state-of-the-art to meet the mission performance specifications.

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